REMARKS

Claims 1-30 are currently pending in the application. Claims 2-13 have been withdrawn from consideration. By this amendment, claims 1 and 14 are amended for the Examiner's consideration. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each .

In the specification, the paragraphs beginning at page 5, line 23, and page 12, line 23, have been amended to correct typographical errors.

The Examiner has rejected claims 1, 14-19 and 22-30 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,273,921 to Neudeck et al. ("Neudeck"). As described in the background section of the present invention, improved FET performance can be obtained by placing gates on multiple sides of an FET channel, provided the silicon is thin enough to be fully depleted (page 2, lines 6-8). However, the prior art fabrication schemes "have relied upon lithographically defined silicon channels and long, confined lateral epitaxial growth" (page 5, lines 24-25). Horizontal double-gated structures are difficult to fabricate because alignment of the top and bottom of the gates cannot be achieved within the desired tolerances with state of the art lithographic equipment, and because the layers between the top and bottom gates frustrate self-aligning techniques (page 2, lines 22-26). Note that the Neudeck reference describes a methodology for alignment of gates. Lithographically defined gates are the simplest, but fail to achieve silicidation of thin diffusions, fabrication of the wraparound gate without misalignment, and fabrication of sufficiently narrow diffusions (page 5, lines 2-14).

The invention, as summarized at page 10, lines 19-24, overcomes these difficulties and provides

> "a very thin diffusion region using a known technique for growing epitaxial regions to form the very thin channel and has the advantages of providing much tighter tolerances on channel thickness than a lithographically defined

> channel which can be maintained by selective etching and that epitaxial growth is not complicated by the presence of thin confining layers."

This is accomplished, as summarized at page 10, lines 13-18, by the steps of

> "forming silicon layers on a substrate. Next, epitaxial channels are formed on a side surface of the silicon layers, with one side wall of the channels therefore being exposed. The silicon layers are then removed, thereby exposing a second sidewall of the epitaxial channels. Source and drain regions are then formed, coupled to ends of the epitaxial channels. Finally, a gate is formed over the epitaxial channels."

The Neudeck reference is related to the present invention, because it concerns fabrication of a dual-gated SOI FET. However, Neudeck is a 1993 patent reflecting prior art technology which is concerned with a channel thickness of 0.1 μm (col 4, line 45), significantly larger than the scale of the channels in the present invention. It would be surprising if Neudeck disclosed the techniques required by the present invention, and upon careful examination it is clear that Neudeck makes no such disclosure. Even a casual reading of Neudeck (col 5, line 1 to col 8, line 49; Figs. 1A-1H, 2A-2D, 3A-3J) discloses that the fabrication method of Neudeck bears very little relation to that of the present invention. It should be noted that in Neudeck the fabrication of the channel – which figures prominently in the present invention, in order to achieve "much tighter tolerances on channel thickness" (page 6, lines 21-22) – is observed but not focused on. The main focus of Neudeck is the independently controllable and self-aligned gates (col 3, lines 19-49).

The Examiner, notwithstanding the foregoing observations, maintains that Neudeck is not only relevant but that Neudeck anticipates the claimed invention, including claim 1. However, the arguments adduced by the Examiner appear to contain speculation not supported by the Neudeck reference. In particular, the Examiner cites Fig. 3F and a discussion in Neudeck at col. 7, line 67, to col. 8, line 3, as corresponding to the element of claim 1 of "removing a channel on a first side of the layer and then removing the layer, thereby exposing a second sidewall of the channel formed on the second side of the layer." The claim language may be

understood by reference to Fig. 2C (showing the formed epitaxial layers 204 on either side of silicon layer 110), Fig. 3B (showing spacer 302 protecting a side of one 204 layer from attack), and Fig. 4B (showing the situation after removal of the other 204 layer and removal of silicon layer 110, where the second side of the first 204 layer is exposed). By contrast, the cited material in Neudeck shows the etching out of amorphous silicon regions 52A and 44 (as shown in Fig. 3E) to form a cavity 56 (as shown in Fig. 3F). There is shown insulating layers (e.g. 43) and oxide sidewalls (e.g. 50), but no indication of a channel on either side of the silicon layer that is removed, nor of removal of a channel on one side. Thus it does not appear that what is shown in Neudeck corresponds to what is shown and claimed in the invention with regard to the element of "removing." Similarly, the description in Neudeck allegedly corresponding to the claim element "forming a second channel in place of said removed channel" is not in correspondence. What is described is an epitaxially grown monocrystalline silicon replacement for the amorphous silicon removed earlier, but since the removed silicon fails to show the claimed relationship to the retained channel (i.e. the two channels in the claimed invention had been formed on either exposed side surfaces of the formed layer), it cannot correspond to the claimed removed channel. Similar comments apply to claim 14, which describes in different language the same method shown in connection with Figs. 2C, 3B and 4B, as above. Therefore, Neudeck is not a valid §102 reference against claims 1 or 14. Nonetheless, the language of claims 1 and 14 has been amended to more closely track what is shown in the figures and described in the specification.

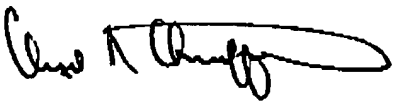
The Examiner has rejected claims 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Neudeck as applied to claims 14-19 and 22-23. However, since claims 20 and 21 depend from claim 14, shown above to be in allowable form, claims 20 and 21 are also allowable.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1and 14-30 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: clyde@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account 09-0456 (IBM-Burlington).

Respectfully submitted,



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